AMENDMENTS TO THE CLAIMS

Please replace all former listings of the claims with the listing presented below:

1. (Original) An intermediate frequency filter for use in an integrated circuit, comprising:
a first filter stage, the first filter stage including a first LC resonator; and
the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface.

2. (Original) The filter of claim 1, wherein:
the first filter stage further including a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations, the second plurality of data storage locations programmable through the serial control interface.

3. (Original) The filter of claim 2, wherein:
the data storage locations of the second plurality of data storage locations are fuses.

4. (Cancelled)

5. (Previously Presented) The filter of claim 1, wherein:
the first capacitive array includes a first capacitor of a first magnitude coupled in series with a first switch and further coupled in series with a second capacitor of the first magnitude, the first switch controlled by a first fuse of the first plurality of fuses; and
the first capacitive array includes a third capacitor of a second magnitude coupled in series with a second switch and further coupled in series with a fourth capacitor of the second magnitude, the switch controlled by a second fuse of the first plurality of fuses, the combination of the third capacitor, second switch and fourth capacitor coupled in parallel with the combination of the first capacitor, first switch and second capacitor.

6. (Cancelled)

7. (Cancelled)

8. (Original) A circuit formed as part of a single integrated circuit, the circuit comprising:
a first amplifier;
a first oscillator;
a first mixer coupled to the first amplifier and the first oscillator;
a second oscillator;
a second mixer coupled to the second oscillator;
a second amplifier coupled to the second mixer;
a serial control module;
an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator;
the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module;
and wherein the second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer.

9. (Original) The circuit of claim 8, wherein the first filter stage further includes:
a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of data storage locations, the first plurality of data.

10-36 (Cancelled)

37. (Original) The filter of claim 1, wherein at least a capacitor of the LC resonator is part of the integrated circuit.

38. (Original) The filter of Claim 1, wherein the first plurality of programmable data storage locations are programmable through a serial control interface of the integrated circuit.

39. (Original) The filter of Claim 38, wherein the first plurality of programmable data storage locations are programmable through a set of test points of the integrated circuit, the test points of the set of test points not directly connected to pins of the integrated circuit.